CMOS VLSI Design
M.Tech. First semester VTU
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Semiconductor technology overview: Modern VLSI technology uses very complex equipment and sophisticated materials. Starting from the raw semiconductor wafer, integrated circuits require several hundred individual process steps before becoming ready for packaging and electrical testing. The process steps can roughly be classified in two groups:

- Structural processing (etching, deposition, oxidation, etc),
- Thermal processing and doping (ion implantation, annealing, etc).

The first group comprehends the processes that force a change in the material's structure, while the second only a modification in their properties (like the doping profile). As most of the process steps are not performed over the entire wafer, a method to selectively apply them to a certain region of the wafer is necessary. This is done by lithography, not included in either groups, as it is necessary in general. We will describe it in the first p

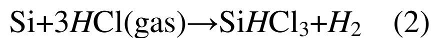
lace.

We will see now how silicon is grown. We start out with a natural form of silicon which is very abundant (and relatively pure); quartzite or SiO_2 (sand). In fact, silicon is one of the most abundant elements on the earth. This is reacted in a furnace with carbon (from coke and/or coal) to make what is known as *metallurgical grade silicon* (MGS) which is about 98% pure, via the reaction

$SiO_2 + 2C \rightarrow Si + 2CO$ (1)

We have seen that on the order of 10^{14} impurities will make major changes in the electrical behavior of a piece of silicon. Since there are about 5×10^{22} atoms/cm^3 in a silicon crystal, this means we need a purity of better than 1 part in 10^8 or 99.999999% pure material. Thus we have a long way to go from the purity of the MGS if we want to make electronic devices that we can use in silicon.

The silicon is crushed and reacted with *H*Cl (gas) to make trichlorosilane, a high vapor pressure liquid that boils at 32°C as in:



$$Si+3HCl(gas)\rightarrow SiHCl_3+H_2 \quad (2)$$

Many of the impurities in the silicon (aluminum, iron, phosphorus, chromium, manganese, titanium, vanadium and carbon) also react with the *H*Cl, forming various chlorides. One of the nice things about the halogens is that they will react with almost anything. Each of these chlorides have different boiling points, and so, by fractional distillation, it is possible to separate out the $SiHCl_3$ from most of the impurities. The (pure) trichlorosilane is then reacted with hydrogen gas (again at an elevated temperature) to form pure *electronic grade silicon* (EGS).

$$SiHCl_3+H_2\rightarrow 2Si+3HCl \quad (3)$$

Although the EGS is relatively pure, it is in a polycrystalline form which is not suitable for device manufacture. The next step in the process is to grow single crystal silicon which is usually done via the *Czochralski*(pronounced "cha-krawl-ski") method to make what is sometimes called CZ silicon. The Czochralski process involves melting the EGS in a crucible, and then inserting a seed crystal on a rod called a puller which is then slowly removed from the melt. If the temperature gradient of the melt is adjusted so that the melting/freezing temperature is just at the seed-melt interface, a continuous single crystal rod of silicon, called a *boule*, will grow as the puller is withdrawn.

Figure 1 is a diagram of how the Czochralski process works. The entire apparatus must be enclosed in an argon atmosphere to prevent oxygen from getting into the silicon. The rod and the crucible are rotated in opposite directions to minimize the effects of convection in the melt. The pull-rate, the rotation rate and the temperature gradient must all be carefully optimized for a particular wafer diameter and growth direction. The <111> direction (along a diagonal of the cubic lattice structure) is usually chosen for wafers to be used for bipolar devices, while the <100> direction (along one of the sides of the cube) is favored for MOS applications. Currently, wafers are typically 6" or 8" in diameter, although 12" diameter wafers (300 mm) are looming on the horizon

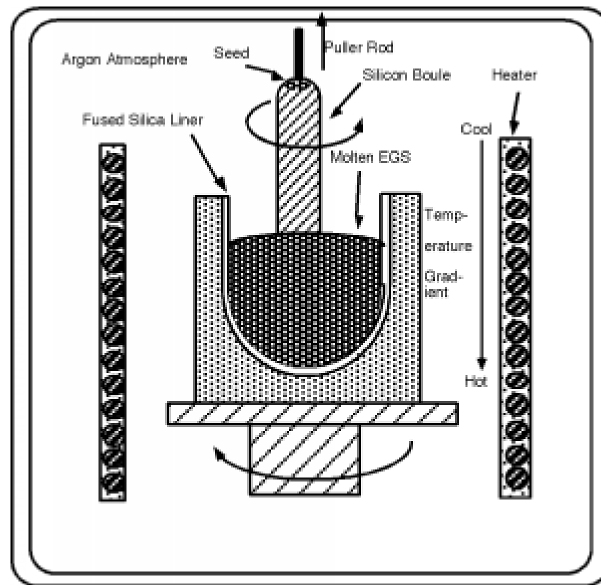


Figure 1: Czochralski process

Once the boule is grown, it is ground down to a standard diameter (so the wafers can be used in automatic processing machines) and sliced into wafers. The wafers are etched and polished, and move on to the process line.

Oxidation: In microfabrication, thermal oxidation is a way to produce a thin layer of oxide (usually silicon dioxide) on the surface of a wafer (semiconductor). The technique forces an oxidizing agent to diffuse into the wafer at high temperature and react with it. The rate of oxide growth is often predicted by the Deal-Grove model. Thermal oxidation may be applied to different materials, but this article will only consider oxidation of silicon substrates to produce silicon dioxide.

Diffusion: The major driving force for the study of diffusion in semiconductor materials is the technological importance of the diffusion process step for integrated circuit (IC) fabrication. Because of undesirable and unpredictable diffusion phenomena, modern process technologies try to reduce diffusion by decreasing the thermal budget. This can be done by reduction of the process temperature or by performing short term annealing processes (RTA) at high temperatures. In all cases the behavior of the diffusion species is anomalous. While lowering the processing temperature does indeed reduce diffusion, enhanced diffusion phenomena became important in the low temperature regimes. As the enhanced diffusion is covered by the dopant self-diffusion at high temperatures, it can become dominant in some low temperature cases. Within RTA processing abnormalities of the dopant profiles are observed and, therefore, conventional diffusion theories fail. There is still a considerable need for understanding diffusion processes in semiconductor materials.

Silicon is the most important substrate material in semiconductor manufacturing. Most of the established diffusion models are focused on silicon, but other materials are also an area of interest for diffusion modeling. For shallow junction fabrication the out-diffusion

of dopants from a doped material layer is important. The two main contenders of silicon in this field are silicides and polycrystalline silicon layers.

Epitaxy: Epitaxy refers to the method of depositing amonocrystalline film on a monocrystalline substrate. The deposited film is denoted as epitaxial film or epitaxial layer. Epitaxial films may be grown from gaseous or liquid precursors. Because the substrate acts as a seed crystal, the deposited film takes on a lattice structure and orientation identical to those of the substrate. This is different from other thin-film deposition methods which deposit polycrystalline or amorphous films, even on single-crystal substrates. If a film is deposited on a substrate of the same composition, the process is called homoepitaxy; otherwise it is called heteroepitaxy.

Deposition: is a chemical process used to produce high-purity, high-performance solid materials. The process is often used in the semiconductor industry to produce thin films. In a typical CVD process, the wafer (substrate) is exposed to one or more volatile precursors, which react and/or decompose on the substrate surface to produce the desired deposit. Frequently, volatile by-products are also produced, which are removed by gas flow through the reaction chamber.

Ion implantation: Ion implantation is a process by which ions are accelerated to a target at energies high enough to bury them below the target's surface. Depending on the application, the acceleration energies can range from a few keV to MeV

Ion implantation was developed as a means of doping the semiconductor elements of integrated circuits. Because of the speed, accuracy, cleanliness and controllability of the process, it has become the standard for this type of work.
In the early 1970s, it was found that ion implantation of metal surfaces could improve their wear, friction and corrosion properties. Ion implantation of specific tools is now preferred over other types of coating technologies because the ion implanted layer doesn't delaminate, doesn't require high processing temperatures to produce, and doesn't add more material on the surface (which would change the size of critical components).

Etching: In wafer fabrication, etching refers to a process by which material is removed from the wafer, i.e., either from the silicon substrate itself or from any film or layer of material on the wafer. There are two major types of etching: dry etching and wet etching.

Wet Etching is an etching process that utilizes liquid chemicals or etchants to remove materials from the wafer, usually in specific patterns defined by photoresist masks on the wafer. Materials not covered by these masks are 'etched away' by the chemicals while those covered by the masks are left almost intact. These masks were deposited on the wafer in an earlier wafer fab step known as 'lithography.'

A simple wet etching process may just consist of dissolution of the material to be removed in a liquid solvent, without changing the chemical nature of the dissolved

material. In general, however, a wet etching process involves one or more chemical reactions that consume the original reactants and produce new species.

A basic wet etching process may be broken down into three (3) basic steps: 1) diffusion of the etchant to the surface for removal; 2) reaction between the etchant and the material being removed; and 3) diffusion of the reaction byproducts from the reacted surface.

Dry etching: The dry etching technology can split in three separate classes called reactive ion etching (RIE), sputter etching, and vapor phase etching.

In RIE, the substrate is placed inside a reactor in which several gases are introduced. A plasma is struck in the gas mixture using an RF power source, breaking the gas molecules into ions. The ions are accelerated towards, and reacts at, the surface of the material being etched, forming another gaseous material. This is known as the chemical part of reactive ion etching. There is also a physical part which is similar in nature to the sputtering deposition process. If the ions have high enough energy, they can knock atoms out of the material to be etched without a chemical reaction. It is a very complex task to develop dry etch processes that balance chemical and physical etching, since there are many parameters to adjust. By changing the balance it is possible to influence the anisotropy of the etching, since the chemical part is isotropic and the physical part highly anisotropic the combination can form sidewalls that have shapes from rounded to vertical. A schematic of a typical reactive ion etching system is shown in the Figure 2 below.

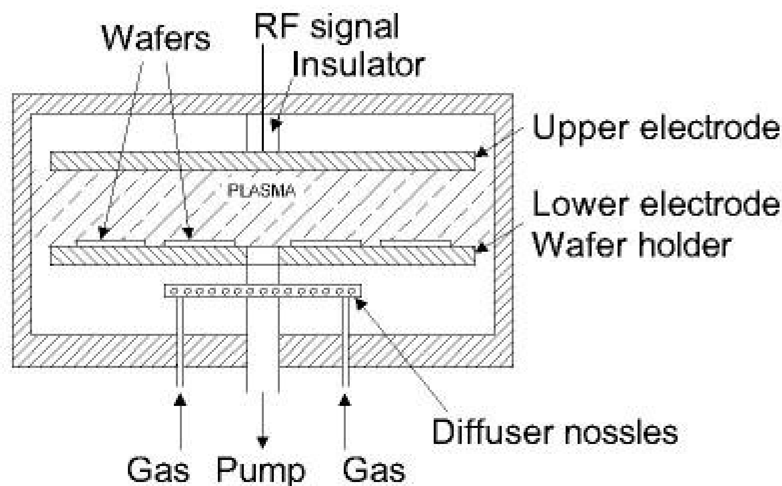


Figure 2 A typical reactive ion etching system

A special subclass of RIE which continues to grow rapidly in popularity is deep RIE (DRIE). In this process, etch depths of hundreds of microns can be achieved with almost vertical sidewalls. The primary technology is based on the so-called "Bosch process", named after the German company Robert Bosch which filed the original patent, where two different gas compositions are alternated in the reactor. The first gas composition creates a polymer on the surface of the substrate, and the second gas composition etches the substrate. The polymer is immediately sputtered away by the physical part of the etching, but only on the horizontal surfaces and not the sidewalls. Since the polymer only dissolves very slowly in the chemical part of the etching, it builds up on the sidewalls and protects them from etching. As a result, etching aspect ratios of 50 to 1 can be achieved. The process can easily be used to etch completely through a silicon substrate, and etch rates are 3-4 times higher than wet etching.

Lithography: Lithography is a process used in microfabrication to selectively remove parts of a thin film or the bulk of a substrate. It uses light to transfer a geometric pattern from a photo mask to a light-sensitive chemical *photo resist*, or simply "resist," on the substrate. A series of chemical treatments then engraves the exposure pattern into the material underneath the photo resist. In complex integrated circuits, for example a modern CMOS, a wafer will go through the photolithographic cycle up to 50 times.

Optical lithography shares some fundamental principles with photography in that, the pattern in the etching resist is created by exposing it to light, either using a projected image or an optical mask. This procedure is comparable to a high precision version of the method used to make printed circuit boards. Subsequent stages in the process have more in common with etching than to lithographic printing. It is used because it affords exact control over the shape and size of the objects it creates, and because it can create patterns over an entire surface simultaneously. Its main disadvantages are that it requires a flat substrate to start with, it is not very effective at creating shapes that are not flat, and it can require extremely clean operating conditions.

N Well CMOS Technology: The n-well CMOS process starts with a moderately doped (with impurity concentration typically less than 1015 cm-3) p-type silicon substrate. Then, an initial oxide layer is grown on the entire surface. The first lithographic mask defines the n-well region. Donor atoms, usually phosphorus, are implanted through this window in the oxide. Once the n-well is created, the active areas of the nMOS and pMOS transistors can be defined. The following is the explanation of sequence of steps to be followed for N-Well CMOS Technology.

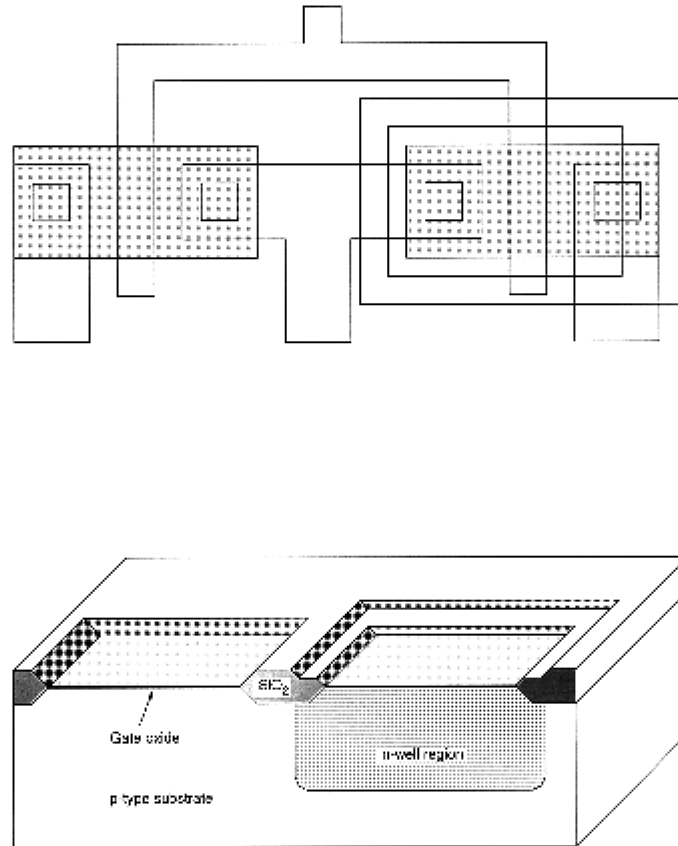


Figure 3 N Well CMOS technology

Following the creation of the n-well region, a thick field oxide is grown in the areas surrounding the transistor active regions, and a thin gate oxide is grown on top of the active regions. The thickness and the quality of the gate oxide are two of the most critical fabrication parameters, since they strongly affect the operational characteristics of the MOS transistor, as well as its long-term reliability.

The polysilicon layer is deposited using chemical vapor deposition (CVD) and patterned by dry (plasma) etching. The created polysilicon lines will function as the gate electrodes of the nMOS and the pMOS transistors and their interconnects. Also, the polysilicon gates act as self-aligned masks for the source and drain implantations that follow this step.

Using a set of two masks, the n+ and p+ regions are implanted into the substrate and into the n- well, respectively. Also, the ohmic contacts to the substrate and to the n-well are implanted in this process step.

An insulating silicon dioxide layer is deposited over the entire wafer using CVD. Then, the contacts are defined and etched away to expose the silicon or polysilicon contact windows. These contact windows are necessary to complete the circuit interconnections using the metal layer, which is patterned in the next step.

Metal (aluminum) is deposited over the entire chip surface using metal evaporation, and the metal lines are patterned through etching. Since the wafer surface is non-planar, the quality and the integrity of the metal lines created in this step are very critical and are ultimately essential for circuit reliability.

The composite layout and the resulting cross-sectional view of the chip, showing one nMOS and one pMOS transistor (built-in n-well), the polysilicon and metal interconnections. The final step is to deposit the passivation layer (for protection) over the chip, except for wire-bonding pad areas.

The patterning process by the use of a succession of masks and process steps is conceptually summarized in Figure 3. It is seen that a series of masking steps must be sequentially performed for the desired patterns to be created on the wafer surface.

Similar sequence holds good for P Well CMOS Technology also, but in complemented manner (N replaced by P and P replaced by N).

Twin-Tub (Twin-Well) CMOS Process

This technology provides the basis for separate optimization of the nMOS and pMOS transistors, thus making it possible for threshold voltage, body effect and the channel transconductance of both types of transistors to be tuned independently. Generally, the starting material is a n+ or p+ substrate, with a lightly doped epitaxial layer on top. This epitaxial layer provides the actual substrate on which the n-well and the p-well are formed. Since two independent doping steps are performed for the creation of the well regions, the dopant concentrations can be carefully optimized to produce the desired device characteristics.

In the conventional n-well CMOS process, the doping density of the well region is typically about one order of magnitude higher than the substrate, which, among other effects, results in unbalanced drain parasitics. The twin-tub process (Figure 4) also avoids this problem.

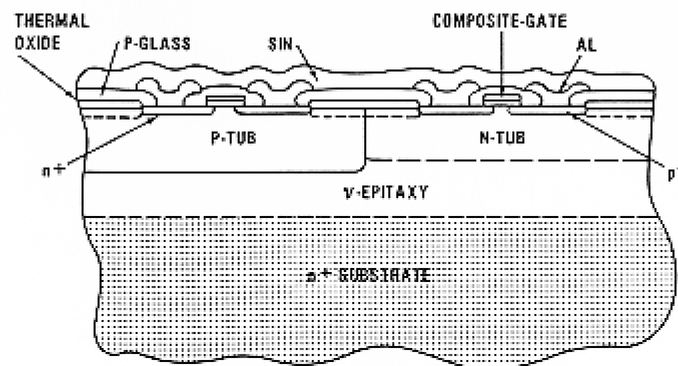


Figure 4 Cross-section of nMOS and pMOS transistors in twin-tub CMOS process

Design rules

The physical mask layout of any circuit to be manufactured using a particular process must conform to a set of geometric constraints or rules, which are generally called layout design rules. These rules usually specify the minimum allowable line widths for physical objects on-chip such as metal and polysilicon interconnects or diffusion areas, minimum feature dimensions, and minimum allowable separations between two such features. If a metal line width is made too small, for example, it is possible for the line to break during the fabrication process or afterwards, resulting in an open circuit. If two lines are placed too close to each other in the layout, they may form an unwanted short circuit by merging during or after the fabrication process. The main objective of design rules is to achieve a high overall yield and reliability while using the smallest possible silicon area, for any circuit to be manufactured with a particular process.

Note that there is usually a trade-off between higher yield which is obtained through conservative geometries, and better area efficiency, which is obtained through aggressive, high- density placement of various features on the chip. The layout design rules which are specified for a particular fabrication process normally represent a reasonable optimum point in terms of yield and density. It must be emphasized, however, that the design rules do not represent strict boundaries which separate "correct" designs from "incorrect" ones. A layout which violates some of the specified design rules may still result in an operational circuit with reasonable yield, whereas another layout observing all specified design rules may result in a circuit which is not functional and/or has very low yield. To summarize, we can say, in general, that observing the layout design rules significantly increases the probability of fabricating a successful product with high yield.

The design rules are usually described in two ways:

- Micron rules, in which the layout constraints such as minimum feature sizes and minimum allowable feature separations, are stated in terms of absolute dimensions in micrometers, or,
- Lambda rules, which specify the layout constraints in terms of a single parameter and, thus, allow linear, proportional scaling of all geometrical constraints.

Lambda-based layout design rules were originally devised to simplify the industry-standard micron-based design rules and to allow scaling capability for various processes. It must be emphasized, however, that most of the submicron CMOS process design rules do not lend themselves to straightforward linear scaling. The use of lambda-based design rules must therefore be handled with caution in sub-micron geometries.

Below, we present a sample set of the lambda-based layout design rules devised for the MOSIS CMOS process and illustrate the implications of these rules on a section a simple layout which includes two transistors (Figure 5).

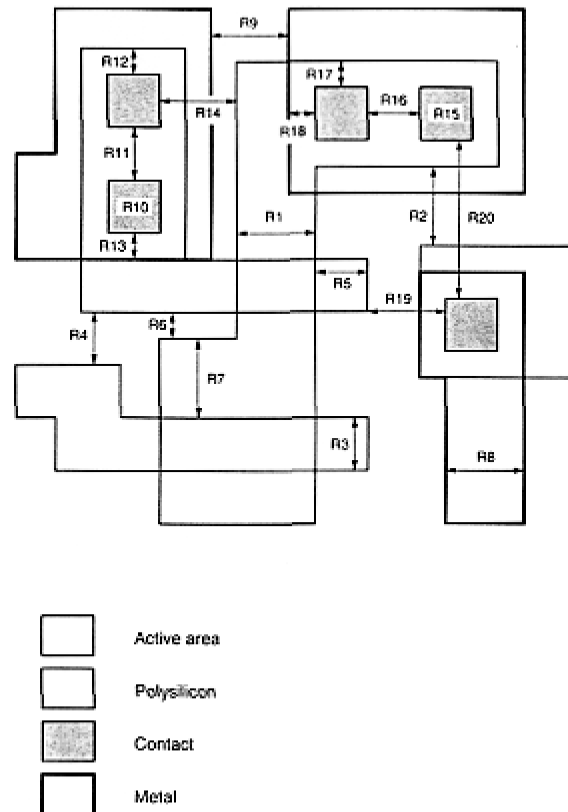


Figure 5 Illustration of some of the typical MOSIS layout design rules listed above

Stick diagrams: The initial phase of layout design can be simplified significantly by the use of stick diagrams - or so-called symbolic layouts. Here, the detailed layout design rules are simply neglected and the main features (active areas, polysilicon lines, metal lines) are represented by constant width rectangles or simple sticks. The purpose of the stick diagram is to provide the designer a good understanding of the topological constraints, and to quickly test several possibilities for the optimum layout without actually drawing a complete mask diagram. In the following, we will examine a series of stick diagrams which show different layout options for the CMOS inverter circuit.

The first two stick diagram layouts shown in Figure 6 are the two most basic inverter configurations, with different alignments of the transistors. In some cases, other signals must be routed over the inverter. For instance, if one or two metal lines have to be passed through the middle of the cell from left to right, horizontal metal straps can be used to access the drain terminals of the transistors, which in turn connect to a vertical Metal-2 line. Metal-1 can now be used to route the signals passing through the inverter. Alternatively, the diffusion areas of both transistors may be used for extending the power and ground connections. This makes the inverter transistors transparent to horizontal metal lines which may pass over.

The addition of a second metal layer allows more interconnect freedom. The second-level metal can be used for power and ground supply lines, or alternatively, it may be

used to vertically strap the input and the output signals. The final layout example in Figure 6 shows one possibility of using a third metal layer, which is utilized for routing three signals on top.

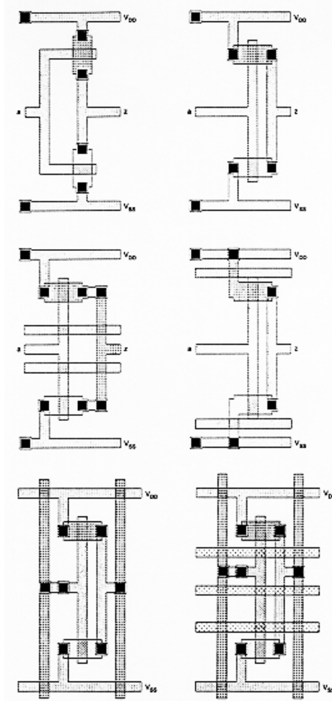


Figure 6 Stick diagrams showing various CMOS inverter layout options

Technology scaling: Scaling is reduction of the dimension of different parameters of MOSFET to achieve the following.

- Increase device packing density.
- Improve speed or frequency response (1/L)
- Improve current drive (Transconductance Gm)
- Decrease Power consumption

Types of scaling:

1) **Constant field scaling** – Requires to reduce power supply voltage with the reduction of feature size. The electric field across the gate-oxide does not change when the technology is scaled.

2) **Constant voltage scaling** – Increasing electric field leads to velocity saturation , mobility degradation , sub threshold leakage

If the power supply voltage is maintained constant the scaling is called constant voltage. In this case, the electric field across the gate-oxide increases as the technology is scaled down.

Limiting factors of scaling:

1) Hot Carrier Effect
2) Punch Through
3) Drain Induced Barrier Lowering (DIBL)
4) Gate Induced Barrier Lowering (GIBL)

Circuit elements - resistor , capacitor, interconnects, sheet resistance & standard unit capacitance concepts, scaling of MOS circuits, delay unit time, inverter delays , driving capacitive loads, propagate delays, MOS mask layer, *stick diagram*, *design rules and layout*.

- Wire Resistance
- Wire Capacitance
- Wire RC Delay
- Repeaters

Chips – majority of wires called *interconnects*

- Transistors are little things with/under the wires
- Many layers of wires

Wires are as important as transistors

- Speed
- Power
- Noise

- Alternating layers run orthogonally = *resistivity* (W*m) $R = \frac{\rho}{t}\frac{l}{w}$
- r = *resistivity* (W*m) $R = \frac{\rho}{t}\frac{l}{w} = R\ \frac{l}{w}$
- Ro = *sheet resistance* (W/o) why?
  - o is a dimensionless unit.
- Count number of squares
  - R = Ro * (# of squares)

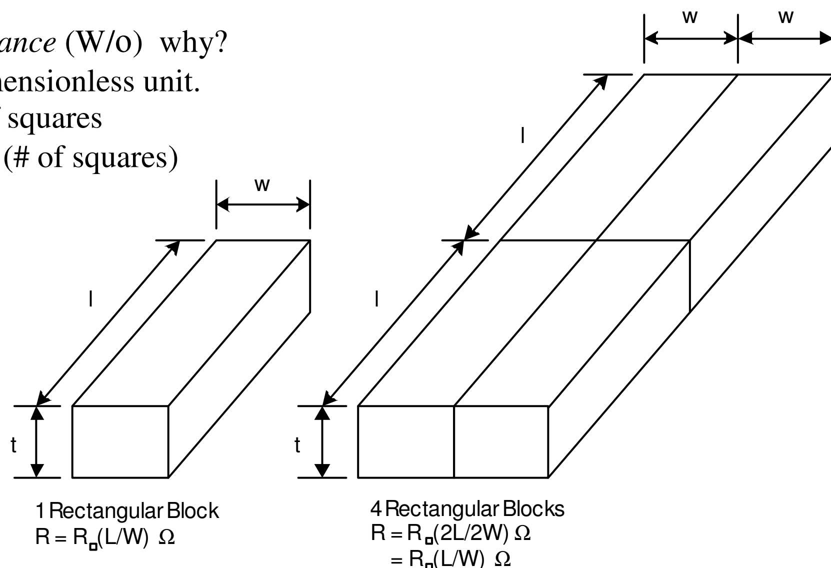


Figure 7 Sheet resistance calculation

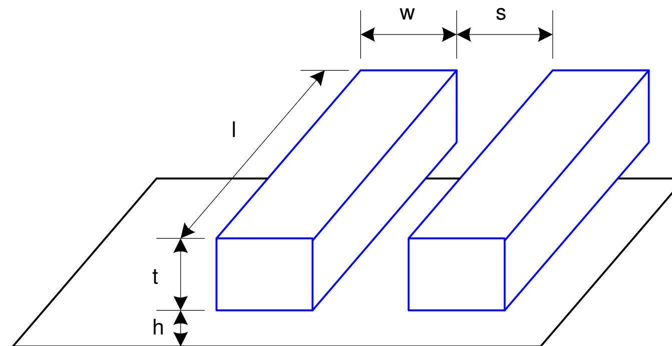


Figure 8 Sheet resistance

Wire capacitance:

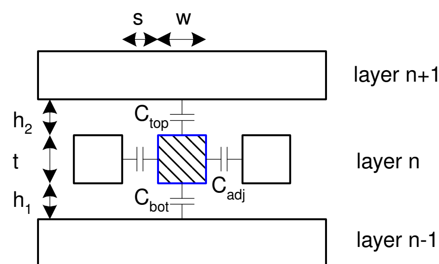


Figure 9 wire capacitance

- Parallel plate equation: C = ϵA/d
  - Increasing area (W, t) increases capacitance
  - Increasing distance (s, h) decreases capacitance
- Dielectric constant
  - e = kϵ0
- ϵ0 = 8.85 x 10-14 F/cm
- k = 3.9 for SiO2
- ϵox = 4 F/µm2
- Area Capacitance - pF/ um2
- Processes are starting to use low-k dielectrics
  - k ≈ 3 (or less) as dielectrics use air pockets
- Standard unit for a technology node is the gate - channel capacitance of the minimum sized transistor (2λ x 2λ), given as □Cg.

- This is a 'technology specific' value
- For a feature size square gate, τ = Rs x □Cg

- i.e for 5µm technology, τ = 104 ohm/sq x 0.01pF = 0.1ns
- Because of effects of parasitics, delay is typically of the order of 0.2 - 0.3 ns

- Diffusion capacitance is very high (about 2 fF/mm)
    - Comparable to gate capacitance
    - Diffusion also has high resistance
- Polysilicon has lower C but high R
    - Used for transistor gates
    - Occasionally used for very short wires between gates

Scaling of Transistors:

- Unit transistor (1X) Scaled 2X, 4X …

- The scaling variables are:

    - Supply voltage: Vdd $\rightarrow$ Vdd / α
    - Gate length: L $\rightarrow$ L / α
    - Gate width: W $\rightarrow$ W / α
    - Gate-oxide thickness: tox $\rightarrow$ tox / α

- Resistance of track R ~ L / wt
- R (scaled) ~ (L / α) / ((w/ α)* (t /α))
- R(scaled) = αR
- Resistance increases with scaling

- Time constant of track connected to gate,
  T = R * Cg
- T(scaled) = α R * Cg/ α = R*Cg
- T is un-scaled!
- Therefore delays in tracks don't reduce with scaling
- Cross talk between connections gets worse because of reduced spacing

- **Interconnect scaling:**
    - Higher densities are only possible if the interconnects also scaled.
    - Reduced width $\rightarrow$ increased resistance
    - Denser interconnects $\rightarrow$ higher capacitance
    - To account for increased parasitics and integration complexity more interconnection layers are added:
        - thinner and tighter layers $\rightarrow$ local interconnections
        - thicker and sparser layers $\rightarrow$ global interconnections and power
- Higher resistance and capacitance leads to higher RC delay

CMOS Inverter Switching Characteristics

Definitions:

- Rise time tr = time required for a node to charge from the 10% point to 90% point
- Fall time tf = time required for a node to discharge from 90% to 10% point
- Delay time td = delay from the 50% point on the input to the 50% point on the output
- Falling delay tdf = delay time with output falling
- Rising delay tdr = delay time with output rising

The Figure 1 depicts the above definitions.

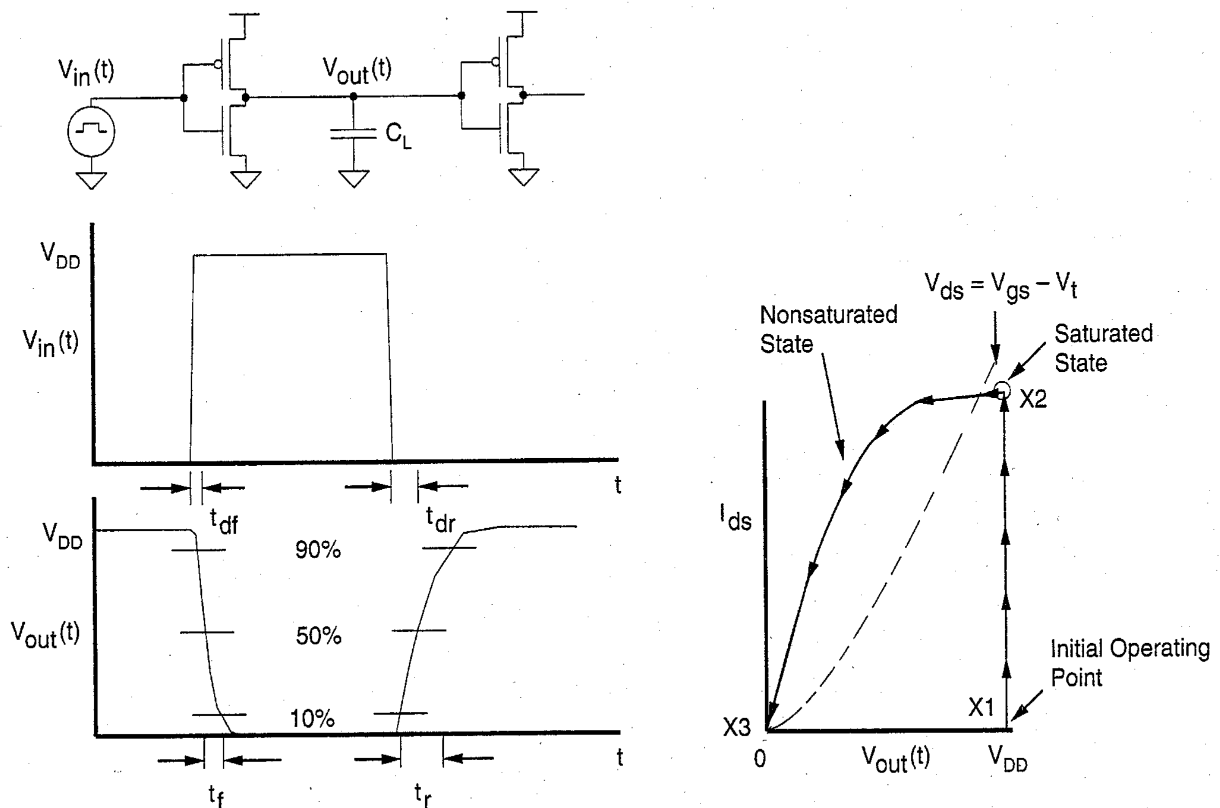
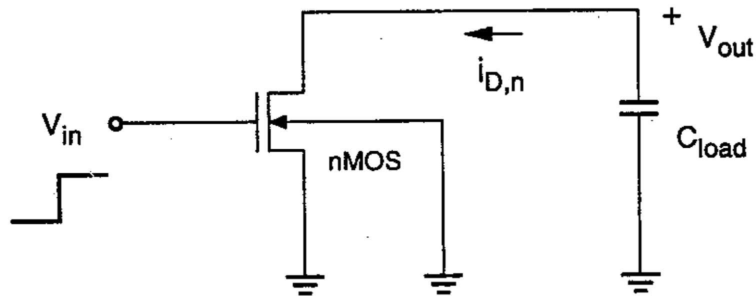


Figure 10 Inverter switching characteristics

Delay Time Derivation: NMOS Discharging Cload:



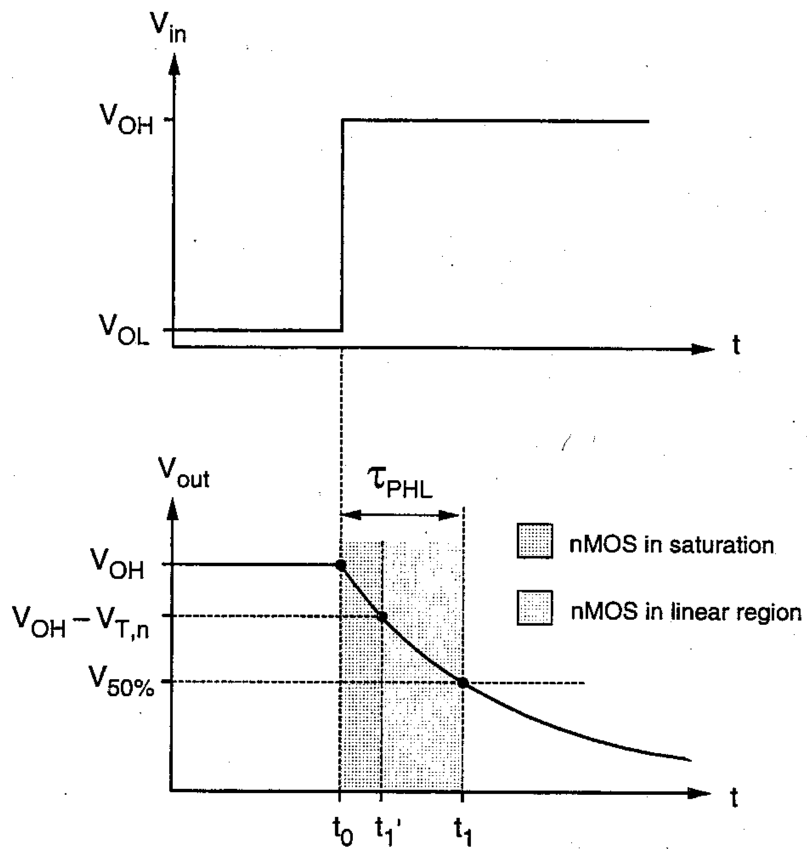


Figure 11 Fall time calculation

- Assume Vin switches abruptly from VOL to VOH (VOL = 0 and VOH = VDD for CMOS)
- We are interested in the delay time for Vout to fall from VOH to the 50% point, i.e. to the value 0.5 x (VOH + VOL), = ½ VDD for CMOS
-
    - For Vout between VOH and VOH – VTN, the NMOS is in saturation
        - Integrate Cload dv = I dt between to and t1'
        - **IDS = ½ kn (Vin – VTN)2**
        - **t1' – to = 2 Cload VTN/kn (VOH – VTN)2**
    - For Vout between VOH – VTN and VOL, the NMOS is in the linear region
        - Integrate Cload dv = I dt between t1' and t1
        - **IDS = kn VDS (VGS – VTN – ½ VDS)**

Summing the two delay components from the previous chart, we obtain the expression (at left) for the propagation delay (high-to low) for an NMOS transistor discharging CL

For CMOS, VOH = VDD and VOL = 0, so the propagation delay (output falling) becomes the expression shown (at left)

A similar expression (left) is obtained by considering the derivation of charging Cload with the PMOS transistor when the input abruptly falls from VDD to 0 and the output rises (low-to-high propagation delay)

$$t_1 - t_1' = \frac{C_{load}}{k_n\left(V_{OH} - V_{T,n}\right)} \ln\left(\frac{2\left(V_{OH} - V_{T,n}\right) - V_{50\%}}{V_{50\%}}\right)$$

$$\tau_{PHL} = \frac{C_{load}}{k_n\left(V_{OH} - V_{T,n}\right)}\left[\frac{2\,V_{T,n}}{V_{OH} - V_{T,n}} + \ln\left(\frac{4\left(V_{OH} - V_{T,n}\right)}{V_{OH} + V_{OL}} - 1\right)\right]$$

$$\tau_{PHL} = \frac{C_{load}}{k_n\left(V_{DD} - V_{T,n}\right)}\left[\frac{2\,V_{T,n}}{V_{DD} - V_{T,n}} + \ln\left(\frac{4\left(V_{DD} - V_{T,n}\right)}{V_{DD}} - 1\right)\right]$$

$$\tau_{PLH} = \frac{C_{load}}{k_p\left(V_{DD} - |V_{T,p}|\right)}\left[\frac{2|V_{T,p}|}{V_{DD} - |V_{T,p}|} + \ln\left(\frac{4\left(V_{DD} - |V_{T,p}|\right)}{V_{DD}} - 1\right)\right]$$

The above expressions for propagation delay can be reduced to the following simplified form by defining n = VTN/VDD for falling output (n = |VTP|/VDD for rising output), and β= βN for falling output (β= βP for rising output) :

τP = k CL/βVDD where **k = [2n/(1-n) + ln (3 – 4n)]/[1-n] = 1.61 for n = 0.2**

CMOS Inverter Fall Time & Rise Time Derivation

Refer Figure 12.

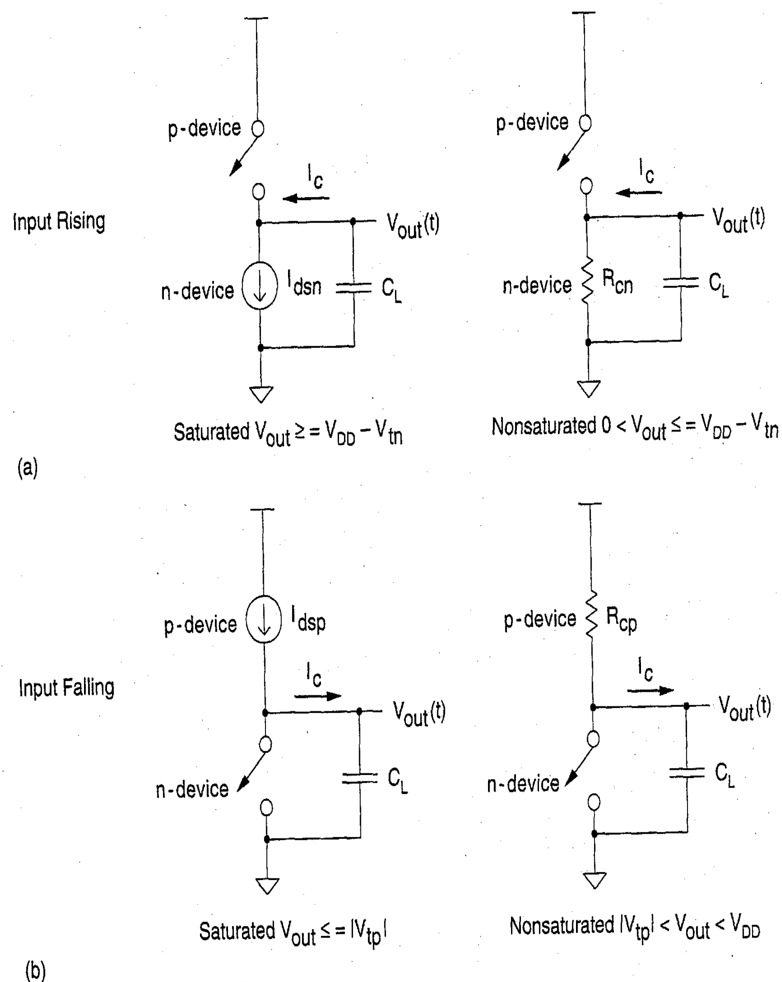


Figure 121 Fall and Rise Time calculations

Discharge Transient: (p device OFF)

– N Saturation region (0.9Vdd>vout>Vdd-Vtn)

$CLdv/dt + ½ βn (Vdd – Vtn)2 = 0$

$t1 = 2CL(Vtn – 0.1Vdd)/βn(Vdd – Vtn)2$

– N Linear Region (Vdd-Vtn>vout>0.1Vdd)

$CLdv/dt + βn v (Vdd – Vtn – 0.5 v) = 0$

$t2 = (CL/βnVdd)[\{ln (19-20n)\}/\{1-n\}]$ where $n = Vtn/Vdd$

– The combined fall time tf is given by

$tf = k CL/βnVdd$ where

$k = [2/(1-n)][(n-0.1)/(1-n) + 0.5 ln(19-20n)]$ $k = \sim 3.7$ for $n = Vtn/Vdd = 0.2$

Charging Transient: (n device OFF)

- Due to the symmetry of CMOS, a similar expression is obtained for rise time where n is replaced by $p = |Vtp|/Vdd$
- Equal CMOS rise and fall times requires $βn = βp$ due to the difference in e & h mobilities.

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