DIGITAL SYSTEM DESIGN

Course Code	: **18EC34**	CIE Marks : 40
Lecture Hours/Week : 03		SEE marks : 60
Total Number of Lecture Hours : 40 (8 Hours / Module)		Exam Hours : 03
CREDITS – 03		

Course Learning Objectives: This course will enable students to:

- Illustrate simplification of Algebraic equations using Karnaugh Maps and Quine-Mc Clusky Techniques.
- Design Decoders, Encoders, Digital Multiplexer, Adders, Subtractors and Binary Comparators.
- Describe Latches and Flip-flops, Registers and Counters.
- Analyze Mealy and Moore Models.
- Develop state diagrams Synchronous Sequential Circuits.
- Appreciate the applications of digital circuits.

Module – 1

Principles of combinational logic: Definition of combinational logic, canonical forms,

Generation of switching equations from truth tables, Karnaugh maps-3,4,5 variables, Incompletely specified functions (Don't care terms) Simplifying Max term equations, Quine-McCluskey techniques – 3 & 4 variables

(Text 1 - Chapter 3) **L1, L2, L3**

Module – 2

Analysis and design of combinational logic: Decoders, Encoders, Digital multiplexers, Adders and subtractors, Look ahead carry, Binary comparators. **(Text 1 - Chapter 4)**

Programmable Logic Devices, Complex PLD, FPGA.

(Text 3 - Chapter 9, 9.6 to 9.8) **L1, L2, L3**

Module -3

Flip-Flops and its Applications: Basic Bistable elements, Latches, The master-slave flip-flops (pulse-triggered flip-flops): SR flip-flops, JK flip-flops, Characteristic equations, Registers, binary ripple counters, and synchronous binary counters.**(Text 2 - Chapter 6)** **L1, L2, L3**

Module -4

Sequential Circuit Design: Design of a synchronous counter, Design of a synchronous mod-n counter using clocked JK, D, T and SR flip-flops.

(Text 2 - Chapter 6)

Mealy and Moore models, State machine notation, Construction of state diagrams. **(Text 1 - Chapter 6)** **L1, L2, L3**

Module -5

Applications of Digital Circuits: Design of a Sequence Detector, Guidelines for construction of state graphs, Design Example – Code Converter, Design of Iterative Circuits (Comparator), Design of Sequential Circuits using ROMs and PLAs, CPLDs and FPGAs, Serial Adder with Accumulator, Design of Binary Multiplier, Design of Binary Divider.

(Text 3 – 14.1, 14.3, 16.2, 16.3, 16.4, 18.1, 18.2, 18.3) **L1, L2, L3**

Course Outcomes: After studying this course, students will be able to:

1. Explain the concept of combinational and sequential logic circuits.
2. Analyze and Design the combinational logic circuits.
3. Describe and characterize flip-flops and its applications.
4. Design the sequential circuits using SR, JK, D, T flip-flops and Mealy & Moore machines.
5. Design applications of Combinational & Sequential Circuits.

Question paper pattern:

- Examination will be conducted for 100 marks with question paper containing 10 full questions, each of 20 marks.
- Each full question can have a maximum of 4 sub questions.
- There will be 2 full questions from each module covering all the topics of the module.
- Students will have to answer 5 full questions, selecting one full question from each module.
- The total marks will be proportionally reduced to 60 marks as SEE marks is 60.

Text Books:

1. John M Yarbrough -Digital Logic Applications and Design, Thomson Learning, 2001.
2. Donald D. Givone —Digital Principles and Design, McGraw Hill, 2002.
3. Charles H Roth Jr., Larry L. Kinney —Fundamentals of Logic Design, Cengage Learning, 7th Edition.

Reference Books:

1. D. P. Kothari and J. S Dhillon, —Digital Circuits and Design, Pearson, 2016.
2. Morris Mano, —Digital Design, Prentice Hall of India, Third Edition.
3. K. A. Navas —Electronics Lab Manual, Volume I, PHI, 5th Edition, 2015.