Chapter 1.

An Overview of VLSI

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An Overview of VLSI

This chapter deals with the basic concepts of VLSI and VLSI DESIGN. A few questions such as what is VLSI/VLSI DESIGN? Why is VLSI? so on and so forth. The chapter looks at the VLSI DESIGN flow and the various options of design that are available for a designer.

1.1 Introduction

The expansion of VLSI is ‘Very-Large-Scale-Integration’. Here, the term ‘Integration’ refers to the complexity of the Integrated circuitry (IC). An IC is a well-packaged electronic circuit on a small piece of single crystal silicon measuring few mms by few mms, comprising active devices, passive devices and their interconnections. The technology of making ICs is known as ‘MICROELECTRONICS’. This is because the size of the devices will be in the range of micro, sub micrometers. The examples include basic gates to microprocessors, op-amps to consumer electronic ICs. There is so much evolution taken place in the field of Microelectronics, that the IC industry has the expertise of fabricating an IC successfully with more than 100 million MOS transistors as of today. ICs are classified keeping many parameters in mind. Based on the transistors count on the IC, ICs are classified as SSI, MSI, LSI and VLSI. The minimum number of transistors on a VLSI IC is in excess of 40,000.
The concept of IC was conceived and demonstrated by JACK KILBY of TEXAS INSTRUMENTS at Dallas of USA in the year 1958. The silicon IC industry has not looked back since then. A lot of evolution has taken place in the industry and VLSI is the result of this. This technology has become the backbone of all the other industries. We will see every other field of science and technology getting benefit out of this. In fact the advancements that we see in other fields like IT, AUTOMOBILE or MEDICAL, are because of VLSI. This being such important discipline of engineering, there is so much interest to know more about this. This is the motivation for this course namely ‘VLSI CIRCUITS’.

1.2 What is VLSI?

VLSI is ‘Very Large Scale Integration’. It is the process of designing, verifying, fabricating and testing of a VLSI IC or CHIP. A VLSI chip is an IC, which has transistors in excess of 40,000. MOS and MOS technology alone is used. The active devices used are CMOSFETs. The small piece of single crystal silicon that is used to build this IC is called a ‘DIE’. The size of this die could be 1.5cmsx1.5cms. This die is a part of a bigger circular silicon disc of diameter 30cms. This is called a ‘WAFR’.

Using batch process, where in 40 wafers are processed simultaneously, one can fabricate as many as 12,000 ICs in one fabrication cycle. Even if a low yield rate of 40% is considered you are liable to get as many as 5000 good ICs. These could be complex and versatile ICs. These could be PENTIUM Microprocessor ICs of INTEL, or DSP processors of TI, each costing around Rs10,000. Thus you are likely to make Rs50 million (Rs5crore) out of one process flow. So there is lot of money in VLSI industry. The initial investment to set up a silicon fabrication unit (called ‘FAB’ in short and also called sometimes as silicon foundry) runs into a few $Billion. In INDIA, we have only one silicon foundry-SCL at Punjab (Semiconductor Complex Ltd., in Chandigarh). Very stringent and critical requirements of power supply, cleanliness of the environment and purity of water are the reasons as to why there are not many FABS in India.
1.3 Complexity
Producing a VLSI chip is an extremely complex task. It has number of design and verification steps. Then the fabrication step follows. The complexity could be best explained by what is known as ‘VLSI design funnel’ as shown in the Fig.1.1.

![VLSI design funnel](image)

1. Money
2. Idea
3. Sand (or Si)
4. CAD Tools
5. Engineers
6. Marketing

Figure1.1 The VLSI design funnel

To set up facilities for VLSI one needs a lot of money. Then the design starts at a highest abstraction in designer’s mind as an initial idea. Engineers using CAD tools further expand this idea. One should have good marketing information also. Then all these are dumped inside the funnel along with a pile of sand as a raw material to get the wonderful item called “the VLSI chip’.

1.4 Design
A state of art of VLSI IC will have tens of millions of transistors. One human mind cannot assimilate all the information that is required to design and implement such complex chip. A design team comprising hundreds of engineers, scientists and technicians has to work on a modern VLSI project. It is important that each member of the team has clear understanding of his or her part of the contribution for the design. This is accomplished by means of the design hierarchy. Any complex digital system may be broken down into gates and memory elements by successively subdividing
the system in a hierarchical manner. Highly automated and sophisticated CAD tools are commercially available to achieve this decomposition. They take very high-level descriptions of system behavior and convert them into a form that ultimately be used to specify how a chip is manufactured. A specific set of abstractions will help in describing the digital system, which is targeted for a VLSI chip. These are well depicted in the Fig.1.2 in a Y-chart. In this figure three distinct domains are marked in three directions in the form letter Y. These domains are Behavioral, Structural and Physical. The behavioral domain specifies what a particular system does. The structural domain specifies how entities are connected together to effect the prescribed behavior (or function). The physical domain finally specifies how to actually build a structure that has the required connectivity to implement the required functionality.

**FIGURE 1.2 The Y-chart**
Each design domain may be specified at a various levels of abstraction such as circuit, logic and architectural. Concentric circles around the center indicate these levels of abstraction. The design hierarchy is shown in the Fig.1.3 in the form of a flow.

FIGURE 1.3 VLSI design flow
The starting point of a VLSI design (of a chip) is the system specifications. The specifications (specs) will provide design targets such as functions, speed, size, power dissipation, cost etc. This is the top level of the design hierarchy. These specifications are used to create an abstract, high-level model. The modeling is
usually done using a high-level hardware description language (HDL), such as VHDL or VERILOG. You have already done a course on digital system design using VHDL in the last semester. Therefore this aspect of modeling a system will not dealt here. Using a HDL compiler the functional simulation is done. The next step in the flow is ‘SYNTHESIS’. Synthesiser is a CAD tool (software), which generates a gate level net list (net list is the description of the logic gates and their interconnections) using the VHDL code as an input.

This forms the basis for transferring the design to the electronic circuit level. In this level of design, the MOS transistors are used as switches, and Boolean variables are treated as varying voltage signals (‘0’ or ‘1’ for digital) in the circuit. Transistors cannot be decomposed further and these are the components, which have to be siliconised. To make a transistor on silicon, one should know the layout details of the same at various integration layer levels. This corresponds to ‘physical design’. The physical design level constitutes the bottom of the design hierarchy. After the design process, the VLSI design project moves on to the manufacturing line. The final result is a finished electronic VLSI chip.

1.5 Design styles

The above said design process is called ‘top-down’ approach. That is because design moves from the highest abstraction level to the lowest level of abstraction namely transistor. The other design approach starts at the transistor (switch) level. Using transistors logic gates are built. Using gates, smaller functional units such as adders, registers and multipliers are built. These are used to build bigger blocks and the system. This approach is known as ‘bottom up’. This is also called the ‘Full – custom’ approach. This approach suits well for small projects. For most of the projects ‘semi-custom’ approach is used. Semi-custom is classified as below:
Semi custom:

- Standard cell based
- Gate array based

In standard cell based design, design details up synthesis will be same as top-down approach. After synthesis, standard cells such as flip-flops, Registers and Multipliers are borrowed from the library to fit (mapping) into the design. These cells would have been custom designed and fully characterized for a given technology. The design cycle time is shorter compared to full custom and the IC is cheaper.

Gate array based design makes use of the transistors’ array or the array of standard gates. Wafers are pre-diffused have M x N array of transistors or Gates in silicon. It is up to the designer to use whatever the number of transistors and connect them in whatever the manner he needs. This is to say that the only design, which is done in this style, is the design of the interconnections, VDD, VSS buses and the communication paths. Masks have to be prepared only for the above said metal layers. Therefore this approach has got a very short design cycle time.

Full custom design as already discussed, stats at the transistor (switch) level. Here the logic style (CMOS, BiCMOS, CCMOS, DYNAMIC CMOS etc) will be decided and the transistor layout details (W/L ratio) will be designed. So this is sometimes called as ‘hand crafted design’. In this approach, silicon area is optimized and the IC comes out to be of high density. The performance is also very high, and the design is very flexible (can easily change). This approach is suitable for large and complex designs. Circuit simulator such as SPICE (Simulation Package with IC Emphasis) and the layout editor such as Magic or Lassi are used.

The design approach using FPGAs (Field Programmable Gate Array) could also be shown under semi custom approach. You have learnt about FPGAs in the last semester under the course...
‘Digital system design using VHDL’ (Roth’s text book). FPGAs are off the shelf readily available CMOS VLSI ICs. These ICs have to be programmed (configured) to suit the designer’s requirement. There are 2 levels of programmability; one at the intra CLB level and the second at the inter CLB level. The I/Os also have to be programmed. The front end design can be done using third part tools but one has to use the vendor specific tools for the back end to generate BIT file (analogous to the GDS-II TAPE step of full custom design approach). The bit file is down loaded to a chosen FPGA. This programmed chip has to be interfaced with other components to finish the PCB card. Many such cards will give you a complete system. This is highly suited for proto typing of systems. As there is no fabrication step (a major step), this design cycle time is shortest among all the approaches. Only draw back is that the designer may not be able to use the resources on the chip to the full extent.

1.6 Concept
VLSI should be thought of as a single discipline that deals with the conception, design and manufacture of complex ICs. Carver Mead is the gentle man who did pioneering work towards VLSI in 1970s. He came out with the standard definition with regard to the formation of a MOS transistor on silicon, which states that ‘when polysilicon cuts across the diffusion, a transistor is formed at the intersection’. Thus he observed that the digital IC could be viewed as a set of geometrical patterns (polygons) on every layer that is going to be integrated on the silicon surface. Thus an IC will comprise of innumerable polygons of conducting (metal and polysilicon), semi conducting (silicon) and non-conducting (insulator such as SiO2) layers at various levels of integration. Groups of patterns represent different logic functions and these are replicated through out the IC. Thus the complexity is broken down using the concept of repeated patterns that were fitted together in a structured manner.

In VLSI two units are quite often used. They are micron (1μm = 10-4 cm = 10-6 meter) and Angstrom (1Å = 10-8 cm=10-10 meter). If the channel length of a transistor = 2λ = 0 .18μm, then
we refer that technology to a 0.18μ technology. The size of the transistor has been reducing ever since the concept of IC was conceived since 1958. In 1970 Gordon Moore predicted the growth of microelectronics in terms of number of transistors that could be fabricated on a chip. He projected that the number of transistors would get doubled every 18 to 24 months. This has been established as ‘MOORE’S LAW’. The silicon industry is facing a tough challenge to keep the pace with the law. On the other hand it is not possible to manufacture a functional design because of defects in the silicon crystal structure that cannot be avoided. The larger the area of the circuit, the higher the probability that a defect will occur. Even a single bad transistor or connection (because of the defect) would make the chip unusable. Therefore the philosophy is to keep the overall size of the chip small.

1.7 Summary
Chapter 2

Logic Design with MOSFETs

2.1 Ideal Switches and Boolean Equations
2.2 MOSFETs as Switches
2.3 Basic Logic Gates in CMOS
2.4 Complex Logic Gates in CMOS
2.5 Transmission Gate circuits
2.5 Clocking and Dataflow Control
2.6 Summary
2.7 Problems
2.8 References
Whole of the digital IC technology revolves around the digital signal. In a digital signal mostly we will have two voltage levels, a high and a low level. These can be easily obtained using ideal switches. This chapter looks at the ideal switches and their series parallel connections from the point of the output and the Boolean operations performed. Later on these switches are mapped by MOS switches from the point of building logic gates as the logic gates are the basic building blocks for VLSI. This chapter looks at the possibility of building standard blocks based on switch logic and restoring logic.

### 2.1 Ideal switches and Boolean operations

Logic gates are implemented using a set of controlled switches. Depending upon the nature of signal with which the switch is controlled, we have two types of switches. They are (a) assert-high controlled and (b) assert-low controlled switches. The situation for the open and closed conditions of the assert –high switch is shown in Fig.2.1

![Figure 2.1 Characteristic of an assert-high switch](image)

Now let us as to how do two switches connected in series and parallel behave for a given input. The behavior is illustrated in Fig. 2.2.and Fig 2.3. The output depends on the control voltages $a$ and $b$.

![Figure 2.2 Series connected switches](image)
The behavior of assert-low switches connected in series and parallel can be shown to be as follows:

The Boolean expression for the two assert-low switches connected in series is 
\[ y = a \cdot b = a + b \]
This expression is in fact the Boolean expression of a 2 input **NOR** gate. But the switches are assert–low switches, the operation holds good only when \( a=b=0 \). If either \( a \) or \( b \) is 1, the output \( y \) is undefined.

Similarly show that the two assert low switches connected in parallel perform a 2 input **NAND** operation for one or two low inputs.
That is, 
\[ y = \overline{a} + \overline{b} = a \cdot b \]
If both \( a \) and \( b \) are 1 then the output is undefined.

**1.2 MOSFETs as switches**